WHAT IS CLAIMED IS:

1. An apparatus comprising:

an inductor; and

an electrically conductive enclosure electromagnetically shielding the inductor, the electrically conductive enclosure having an aperture at least as large as the inductor, the aperture being substantially centered around a projected surface of the inductor.

2. The apparatus, as recited in claim 1, wherein the aperture is substantially parallel to a plane of current flow in the inductor.

3. The apparatus, as recited in claim 1, wherein the aperture has an approximate diameter determined by adding an approximate outer diameter of the inductor to an approximate inner diameter of the inductor.

4. The apparatus, as recited in claim 1, further comprising:

one or more electrically conductive links extending across the aperture and electrically coupled to the electrically conductive enclosure, the electrically conductive links reducing an effect of electromagnetic signals external to the electrically conductive enclosure on the inductor.

5. The apparatus, as recited in claim 4, wherein the electrically conductive links reduce coupling in the inductor from external sources by approximately 6dB.

6. The apparatus, as recited in claim 4, wherein the electrically conductive links are approximately 5μm wide.

7. The apparatus, as recited in claim 4, wherein the electrically conductive links are formed in the one or more traditional integrated circuit layers.

8. The apparatus, as recited in claim 1, wherein the electrically conductive enclosure includes a top plate, a bottom plate, and sidewalls.

9. The apparatus, as recited in claim 8, wherein the aperture is formed by omission of one of the top and bottom plates of the electrically conductive enclosure.

10. The apparatus, as recited in claim 8, wherein the aperture is formed in the bottom plate.

11. The apparatus, as recited in claim 8, wherein the bottom plate is formed in one or more integrated circuit metal layers.

12. The apparatus, as recited in claim 8, wherein the top plate is formed in a metal layer.

13. The apparatus, as recited in claim 8, wherein the top plate is formed in a redistribution layer.

14. The apparatus, as recited in claim 8, wherein the top plate is formed in a package substrate.

15. The apparatus, as recited in claim 1, wherein the inductor is formed at least partially in one or more metal layers of an integrated circuit die thicker than others of the metal layers.

16. The apparatus, as recited in claim 1, wherein the inductor is formed at least partially in one or more redistribution layers formed on an integrated circuit die.

17. The apparatus, as recited in claim 1, wherein the inductor is formed on an integrated circuit die.

18. The apparatus, as recited in claim 17, wherein a conductor forming the inductor is 10μm wide.

19. The apparatus, as recited in claim 17, wherein the aperture and the inductor are effectively spaced at least 10.25μm apart.

20. A method comprising:

reducing a current induced in an electrically conductive enclosure generated in response to an inductor, the induced current generating an electromagnetic field counteracting an effective electromagnetic field generated by the inductor, the reducing using at least one aperture in the electrically conductive enclosure.

21. The method, as recited in claim 20 further comprising:

reducing an effective aperture utilizing links for generating a current to counteract at least some external electromagnetic signals entering the electrically conductive enclosure through the aperture.

22. The method, as recited in claim 20 further comprising:

providing the inductor on the integrated circuit die with sufficient space with respect to the electrically conductive enclosure to reduce the current induced in the electrically conductive enclosure.

23. A computer-readable medium encoding an integrated circuit product comprising:

an inductor; and

an electrically conductive enclosure electromagnetically shielding the inductor, the electrically conductive enclosure having an aperture at least as large as the inductor, the aperture being substantially centered around a projected surface of the circuit element.

24. A method of manufacturing an integrated circuit product comprising:

forming an inductor; and

forming an electrically conductive enclosure electromagnetically shielding the inductor, the electrically conductive enclosure having an aperture at least as large as the inductor, the aperture being substantially centered around a projected surface of the inductor.

25. The method, as recited in claim 24, further comprising:

forming the aperture substantially parallel to a plane of current flow in the inductor.

26. The method, as recited in claim 24, further comprising:
forming the aperture having an approximate diameter determined by adding an approximate outer diameter of the inductor to an approximate inner diameter of the inductor.

27. The method, as recited in claim 24, further comprising:
forming one or more electrically conductive links extending across the aperture and electrically coupled to the electrically conductive enclosure, the electrically conductive links reducing an effect of electromagnetic signals external to the electrically conductive enclosure on the inductor.

28. The method, as recited in claim 27, wherein the electrically conductive links reduce coupling in the inductor from external sources by approximately 6dB.

29. The method, as recited in claim 27, further comprising
forming electrically conductive links approximately 5μm wide.

30. The method, as recited in claim 27, further comprising
forming the electrically conductive links in the one or more traditional integrated circuit layers.

31. The method, as recited in claim 24, further comprising:
forming the electrically conductive enclosure including a top plate, a bottom plate, and sidewalls.

32. The method, as recited in claim 31, further comprising:
forming the aperture by omitting of one of the top and bottom plates of the electrically conductive enclosure.

33. The method, as recited in claim 31, further comprising:
forming the aperture in the bottom plate.

34. The method, as recited in claim 31, further comprising:

forming one or more integrated circuit metal layers on an integrated circuit die; and

forming the bottom plate in the one or more integrated circuit metal layers.

35. The method, as recited in claim 31, further comprising:

forming a metal on an integrated circuit die; and

forming the top plate in the metal layer.

36. The method, as recited in claim 31, further comprising:

forming a redistribution layer on an integrated circuit die; and

forming the top plate in the redistribution layer.

37. The method, as recited in claim 31, further comprising:

forming a package substrate; and

forming the top plate in the package substrate.

38. The method, as recited in claim 24, further comprising:

forming one or more metal layers on an integrated circuit die thicker than others of the metal layers; and

forming the inductor at least partially in the one or more metal layers.

39. The method, as recited in claim 24, further comprising:

forming redistribution layers on an integrated circuit die; and

forming the inductor at least partially in one or more redistribution layers.

40. The method, as recited in claim 24, further comprising:

forming the inductor using a conductor that is 10μm wide.

41. The method, as recited in claim 24, further comprising:

forming the aperture effectively spaced from the inductor by at least 10.25μm.

42. An apparatus comprising:

means for electrically coupling nodes of an integrated circuit;

means for electromagnetically shielding the coupling means; and

means for reducing current induced in the shielding means in response to the coupling means, the induced current generating an electromagnetic field counteracting an electromagnetic field generated by the coupling means.